Description

P9148 is a power management device used in conjunction with the P9145/P9180 PMIC to either increase the output current capability of integrated power stage buck converter rails or implement extra output rails when connected to the PMIC's standalone controller interface. The device works as a controlled current source that supplies current to the load above what the host PMIC can deliver on its own. Up to four P9148 DPUs may be used in parallel to provide an additional 24A of peak load current capability.

A high-speed 2-wire digital bus connects the P9145/P9180 to the P9148 DPUs to provide control and exchange status information. The device seamlessly integrates into the PMIC eco-system and is transparent from a user point of view.

The P9148 is available in a 4 × 3 mm, 12-ld DFN package. It is guaranteed to operate over the industrial temperature range of -40°C to +85°C.

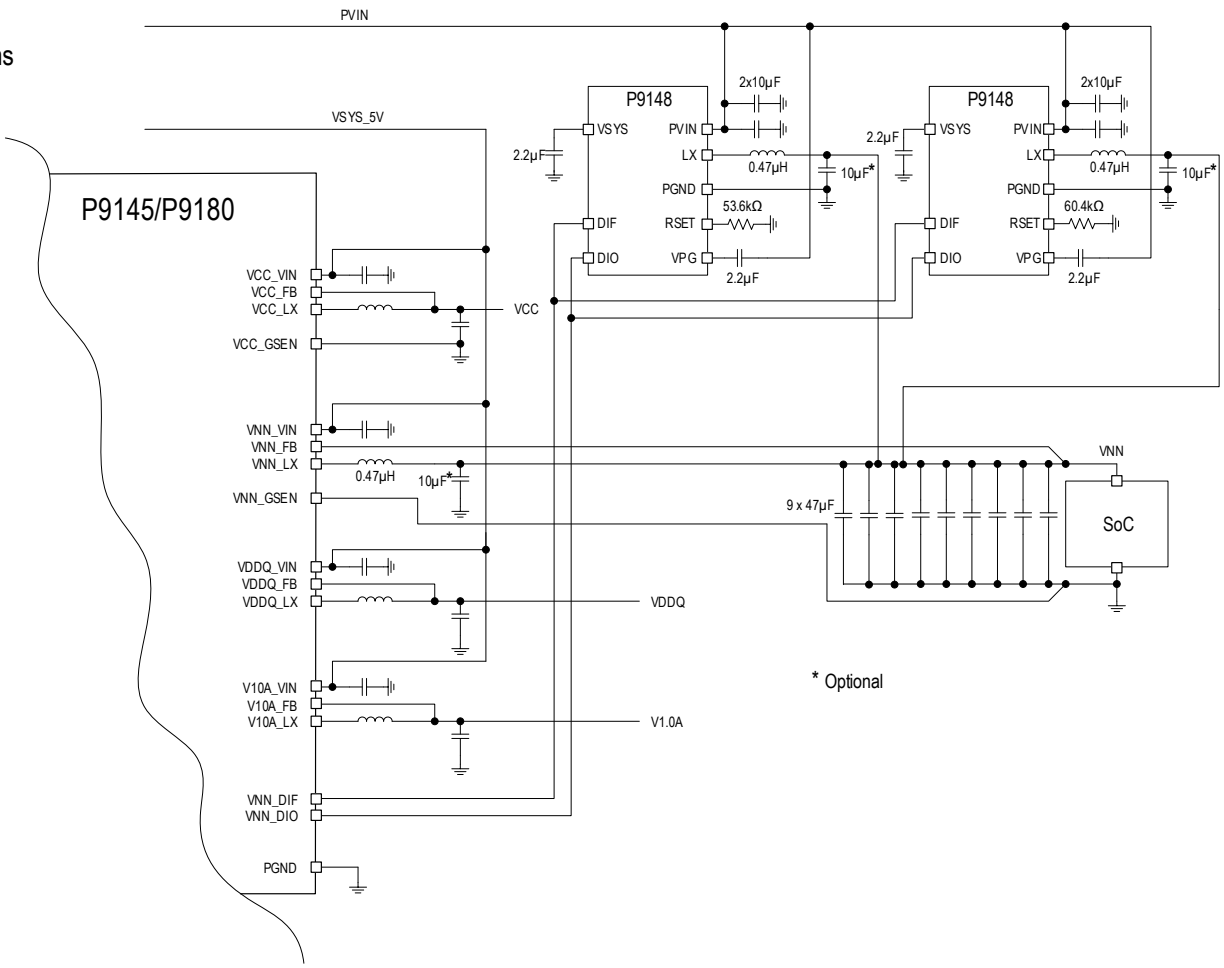
Features

- Operates from a single 4.5V to 8.4V supply
- Peak output current up to 6A
- Switching frequency: 2MHz
- Support for up to 4 DPUs supplying the same rail
- Multiphase output: up to 5 phases configured automatically depending on number of devices
- Output voltage compliance: 0.75V to 3.6V
- 2-wire digital bus interface for device configuration, control, and status exchange with the host PMIC
- -40°C to +85°C ambient operating temperature range
- 3.0 × 4.0 × 0.90 mm 12-DFN package

Typical Applications

- Tablet PCs
- Notebooks
- Embedded systems

Typical Application Circuit including Connection to P9145/P9180 Host PMIC



Contents

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List of Figures

List of Tables

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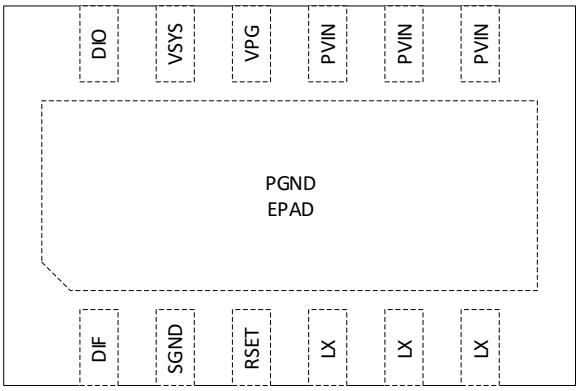
1. Pin Assignments

Figure 1. P9148 Pin Assignments for 3.0 × 4.0 × 0.90 mm 12-DFN – Top View



2. Pin Descriptions

Table 1. P9148 Pin Descriptions

Pin Number	Name	Type	Description
1	DIF	Input	Digital interface to the host PMIC: 1.8V logic input.
2	SGND	Ground	DIF/DIO signal ground reference: Connect directly to the ground plane.
3	RSET	Analog	RSET resistor connection: Connect to the device identification/configuration resistor.
4, 5, 6	LX	Analog	Switching node inductor connection: Connect to either a 0.47µH or 1µH inductor depending on the application.
7, 8, 9	PVIN	Analog	Power supply input: Connect 2×10µF capacitors directly between the PVIN pins and PGND EPAD (no via). A capacitor can be connected to the ground plane instead when the PVIN supply plane is stacked adjacent to the ground plane. Use at least 4 vias for each capacitor connection.
10	VPG	Analog	High-side regulator output capacitor connection: Connect a 2.2µF capacitor directly between VPG and PVIN pin (no vias).
11	VSYS	Analog	Low-side regulator output capacitor connection: Connect a 2.2µF capacitor directly between VSYS and the PGND EPAD (no vias).
12	DIO	Input/Output	Digital interface to the host PMIC: Bi-directional 1.8V logic input and open-drain output.
EPAD	PGND	Ground	Device ground (EPAD): At least 10 vias should be used to connect the EPAD to the ground plane directly below the device.

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3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the P9148 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Note: All voltages are referred to ground, unless otherwise noted.

Parameter	Conditions	Minimum	Maximum	Units
PVIN Pin		-0.3	9.6	V
VSYS, RSET Pins		-0.3	6.0	V
DIF, DIO Pins		-0.3	2.2	V
LX Pin – DC Voltage	Time > 500ns	-0.3	9.6	V
LX Pin – AC Voltage	Time < 500ns	-1.2	16	V
PVIN Pin to VPG Pin		-0.3	< 6.0	V
ESD Human Body Model (HBM) (All Pins)		-1000	+1000	V
ESD Charge Device Model (CDM) (All Pins)		-500	+500	V

Table 3. Thermal Characteristics

Note: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Symbol	Parameter	Value	Units
θ_{JA}	Thermal Resistance Junction to Ambient	36	°C/W
$\theta_{JC(T)}$	Thermal Resistance Junction to Top of Case [a], [b]	66	°C/W
$\theta_{JC(B)}$	Thermal Resistance Junction to Bottom of Case [a], [b]	0.8	°C/W
T_J	Junction Temperature	-40 to +125	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

[a] The thermal rating is calculated based on a JEDEC standard 4-layer printed circuit board (PCB) with dimensions 101mm x 101mm in still air conditions with 2oz. copper on all four layers, 10 thermal vias at 889µm pitch, 508µm drills connecting to the EPAD, and an extended PCB pad of 760µm.

[b] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

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4. Electrical Characteristics

Table 4. Electrical Characteristics

Note: See Figure 3 for the related components. Conditions: V_{PVIN} = 6V, V_{OUT} = 1V, L = 0.47µH, C_{OUT} = 3 x 47µF, C_{PVIN} = 2 x 10µF, C_{VPG} = 2.2µF, C_{VSYS} = 2.2µF, unless otherwise noted.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{PVIN}	Input Voltage Range		4.5		8.4	V
V_{UV}	Pvin Under-Voltage Lock-Out	PVIN rising threshold	4.35	4.4	4.45	V
		PVIN falling threshold	3.95	4.0	4.05	V
V_{SYS}	Low-Side LDO Output Voltage			4.8		V
V_{PG}	High-Side LDO Output Voltage			V_{PVIN} – 4.8		V
I_{SHDN}	Shutdown Current	DIO = 0V		1	10	µA
I_Q	Quiescent Current	Standby Mode: DIO = HIGH, DIF = LOW		180	210	µA
		Idle Mode: DIO = HIGH, DIF = active, LX not switching		520	600	µA
I_{OP}	Operating Supply Current	Active Mode, switching, no load		18	30	mA
I_{OUT}	Continuous Output Current	T_J < 115°C Guaranteed by design [a]			4.5	A
I_{PULSE}	Maximum Pulse Load Current	Pulse duration < 1ms Pulse duty-cycle < 0.1%		6		A
$R_{(on)}$	High-Side Switch			55		mΩ
	Low-Side Switch			30		mΩ
f_{SW}	Switching Frequency	Set by half of DIF input frequency		0.5 x f_{DIF}		MHz
I_{LIM}	LX Peak Current Limit	Occurs at maximum DIF duty-cycle of 83%	6.0	6.5		A
T_{SD}	Thermal Shutdown Temperature	Guaranteed by design [b]	127	135		°C
t_{SDDLY}	Thermal Shutdown Delay			4		ms
Digital I/O (Informative)						
V_{IL}	LOW Level Input Voltage			0.65		V
V_{IH}	HIGH Level Input Voltage			1.15		V
V_{OL}	DIO Output LOW Voltage	At I_{OL} = 12mA (open-drain output)			0.4	V

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Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_{DG}	Input De-glitch Time			4		ns
f_{DIF}	DIF Input Frequency	Informative only		4.0		MHz
t_{ST}	Device Start-up Time	From DIO assertion		300		µs
D_{MAX}	Maximum Distance from Host to Farthest DPU Device	C_{TRACE} < 80pF		2		ft

[a] Specification set by metal electro-migration limit based on 10yr continuous operation as determined by R3D simulations.

[b] Guaranteed by characterization over 3 wafer lots.

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5. Theory of Operation

5.1 Overview

The P9148 is a power-stage operating as a controlled current-source, and it is used in conjunction with the P9145/P9180 PMIC's switching buck converter rails. The P9148 is used to increase the output current capability of the host PMIC's buck converter rails with an integrated power stage. It is also used by the host PMIC to implement additional buck outputs when connected to the PMIC's standalone controllers. The device communicates with the host PMIC via a proprietary 2-wire digital bus comprising the DIO and DIF signals. Up to four devices can be connected to the bus to provide an additional 24A of output current capability to the voltage rail. A device identification resistor connected to the RSET pin is used by each DPU to select the device ID and configuration that determines the phasing and slope compensation setting of the device. During device start-up, a 12µA current source is applied to the RSET pin. The voltage generated by the resistor is measured by the DPU and decoded to extract the ID and configuration information.

Multiple P9148 ICs combined with the host PMIC have the ability to activate and shed phases seamlessly while continuously supplying the desired current to the load. Other capabilities of the P9148 include:

- Current limit control
- Under-voltage lockout
- Thermal shutdown

5.2 DIO/DIF Interface Description

5.2.1 General

The DIO and DIF bus connects the host PMIC to up to four P9148 DPUs to provide control and exchange status information. A dedicated DIO/DIF pair is utilized for each output rail. The DIO signal is primarily used to convey configuration information and provide the handshake between the host and the DPUs. It also serves as the device master enable as well as the ON/OFF control for individual phases. The DIF signal provides timing and synchronization for DIO data and also controls the output current of the DPUs via duty-cycle modulation. The LX switching frequency is derived from the DIF clock frequency. When the voltage rail is switched-off, the DIF signal is LOW and inactive. When the rail is switched-on and one or more DPUs are active and switching, the DIF clock runs at 4MHz. In the idle condition, when the voltage rail is still enabled but all DPUs have been phase-shed, the DIF clock lowers to 1MHz frequency to save power while maintaining the synchronization that is required to support immediate phase activation during a load step. To ensure robust operation in the presence of noise, interference, and ground bounce, error correction circuitry is employed to ignore glitches, runt pulses, and invalid phase and duty-cycle presented at the DIF input.

5.2.2 Initialization

During initialization, the host first asserts the DIO signal to enable the DPUs. The individual DPUs then start up and immediately read the connected R_{SET} resistor value to determine its phase ID and device configuration. The host PMIC then queries the bus to determine the number of DPUs attached, and individual DPUs respond with their respective IDs. For robustness, the query process is repeated to confirm a consistent response from all DPUs. Once the host has determined the number of DPUs present, the information is broadcast to all DPUs so individual DPUs can configure their phasing appropriately. The phases are distributed evenly across the entire switching period. If multiple DPUs have the same phase ID, then the host will treat them as a single DPU, and those phases will be synchronous.

5.2.3 DIF Signal Integrity Calibration

Depending on the number of DPUs attached, the host automatically configures its DIO and DIF I/O drivers to provide the best signal quality. Varying line capacitance can change the rise and fall times of the DIF clock pulses and distort the perceived duty-cycle of the signal, which represents the output current. To minimize this distortion, the DIF channel is calibrated at start-up and re-calibrated whenever possible to ensure the control transfer function is maintained in each of the DPUs across all bus loading conditions. As a result, the individual DPUs could be located away from the host PMIC, virtually anywhere on the board where space and thermal dissipation allows.

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5.3 Phase Activation and Phase Shedding Control

Individual DPU phases are automatically shut off sequentially, starting with the lowest ID first, as load current demand decreases. When load demand returns, all phases will be switched-on at the same time to minimize the output voltage droop due to the load step. Both current and time hysteresis are built into the phase activation/shedding decision circuitry in the host PMIC to ensure stable operation. Phase activation and phase shedding control are achieved by specific pulse detection on the DIO line. Phase-shedding is not supported when the DPUs are connected to the host PMIC's integrated controller.

5.4 PFM Mode Support

When the P9148 DPUs are connected to converter rails of the P9145/P9180 with integrated power stages (DCD0, DCD1, DCD2), PFM Mode operation is provided by the power stage on board the P9145/P9180, and it occurs at light load after all DPU phases have been shed.

When the DPUs are used in conjunction with the P9145/P9180 PMIC's standalone controllers (DCD3, DCD4), PFM Mode operation is serviced by the DPUs themselves. During PFM operation, the DPUs burst on and off concurrently at intervals controlled by the host PMIC's controller to maintain the output voltage level.

5.5 Thermal Shutdown

Thermal shutdown occurs when the die temperature exceeds 135°C. A 4ms time filter is included to prevent unintended shutdown. Once thermal shutdown occurs, the particular DPU will permanently be disabled until the output voltage rail is power-cycled. Until then, the host PMIC's integrated power stage and remaining DPUs must absorb the extra load current. Thermal shutdown on an individual DPU will not affect the output voltage rail unless the host PMIC over-heats and shuts down as well, or if only one DPU is used in conjunction with the PMIC's integrated controller.

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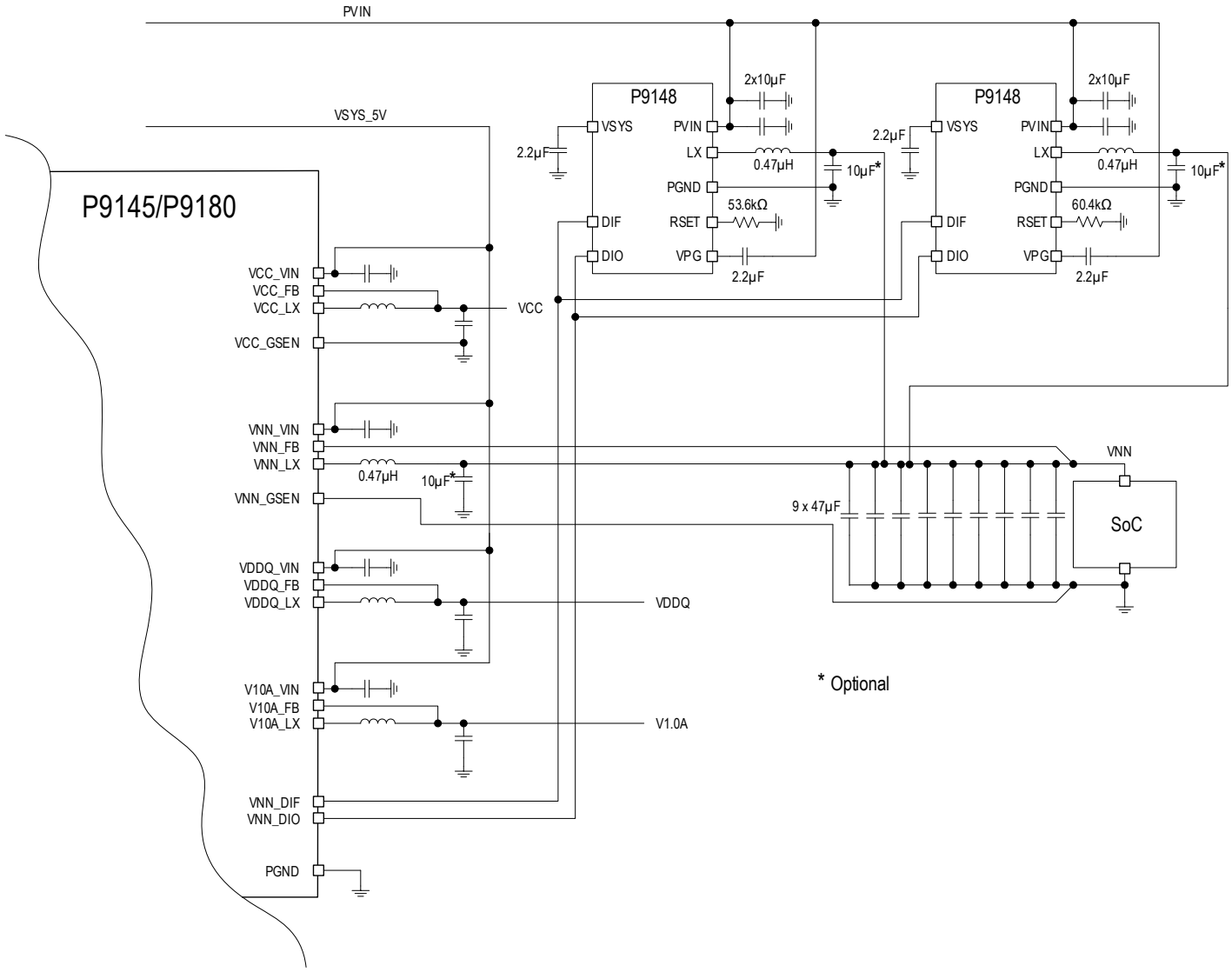
6. Application

6.1 Typical Application Diagram

In Figure 2, the 10µF capacitor placed next to the inductor of each DPU may be omitted if board space is limited and the main output capacitor cluster is within approximately 2 inches away. The inductance value of the LX inductor connected to the DPUs might need to be 1µH in some applications as listed in Table 6. The RSET resistor value of each DPU is usually different and depends on the configuration and phase of the particular DPU as shown in Table 7.

Figure 2. Typical Application Diagram Showing Two P9148s Connected as DPUs to Augment the Output Current Capability of the P9145/P9180 PMIC's VNN Rail



6.2 Bill of Materials (BOM)

Figure 3. Schematic for 5V Input

Note: Option B for L_X in Table 5 is recommended for V_{IN} > 5.5V and V_{OUT} > 3.3V.

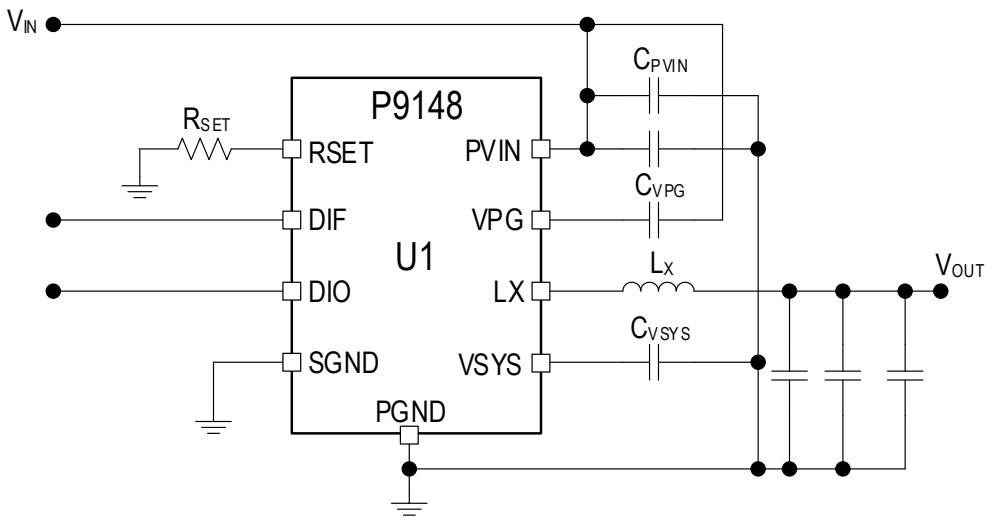


Table 5. Bill of Materials

Designator	Value	Package	Manufacturer P/N	Manufacturer	Quantity
C_{PVIN}	10µF	CAP: 10µF, ±10%, 25V, X7R,1206, 3.2x1.6x1.6mm	C3216X7R1E106K	TDK	2
C_{VPG}	2.2µF	CAP: 2.2µF, ±10%, 10V, X7R, 0603, 1.6x0.8x0.8mm	C1608X7R1A225K	TDK	1
C_{VSYS}	2.2µF	CAP: 2.2µF, ±10%, 10V, X7R, 0603, 1.6x0.8x0.8mm	C1608X7R1A225K	TDK	1
C_{OUT}	47µF	CAP: 47µF, ±10%, 6.3V, X7R, 1210, 3.2x2.5x2.5mm	GRM32ER70J476KE20	Murata	3
L_X (A)	0.47µH	INDUCTOR: 0.47µH, ±20%, 6.5A, SMD, 4.0X4.0X1.2mm	FDSD0412-H-R47M	Toko	1
L_X (B)	1µH	INDUCTOR: 1µH, ±20%, 5.3A, SMD, 4.0X4.0X1.5mm	FDSD0415-H-1R0M	Toko	
R_{SET}	Varies	RES: ±1%, 0.1W, SMD		Any	1
U1	P9148	P9148	P9148NRGI	IDT	1

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7. Design of Components

7.1 Suggested Components and Slope Compensation Setting

Depending on the expected input and output voltage requirement for the application, the recommended inductor and output capacitor values as well as the associated slope compensation setting are provided in Table 6. These component values will provide the best nominal stability and transient response. It is recommended that the 47µF output capacitors for all DPUs be clustered together at the point-of-load where the feedback connection is, with the optional 10µF capacitor placed next to the DPU's inductor to absorb ripple current.

The slope compensation setting is selected by choosing the appropriate R_{SET} resistor value as shown in Table 6.

Table 6. Recommended Component Values and Slope Compensation Setting

V_{OUT} (V)	PVIN (V)	L (µH)	C_O (µF)	Slope Compensation
3.3	4.5 to 5.5	0.47	10 +(3 × 47)	HIGH
3.3	5.6 to 8.4	1.0	10 + (3 × 47)	LOW
< 2V (e.g., 1.8)	4.5 to 8.4	0.47	10 + (3 × 47)	LOW

7.2 Component Selection

If deviation from the recommended components is desired to further optimize the regulator response for a specific application, guidelines are provided in the following section to aid in the component selection process.

7.2.1 Inductor – L

L is the inductor connected to the switch node of the P9148**.** The inductor physical size selection should consider its temperature rise and current saturation for the expected operating conditions. The peak current through the inductor is typically 6.5A. The inductor value chosen should take into account ripple current considerations, which can affect peak current handling capability, efficiency, and board EMI performance.

The inductor ripple current can be calculated from Equation 1:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{f_{SW} L} \times \frac{V_{OUT}}{V_{IN}} \qquad \textbf{Equation 1}$$

where L = Inductor value (µH)

V_{IN} = Input voltage (V)

V_{OUT} = Output voltage (V)

f_{SW} = Switching frequency (MHz)

ΔI_L = Inductor current ripple (A)

For typical applications, as described in Table 4, the ripple current equates to 886mA_{PP}.

For an inductor peak current limit specification of 6.5A, this translates to a maximum load current capability of 6.06A.

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7.2.2 Power Input Capacitor – C_{PVIN}

C_{PVIN} is the power input bypass capacitor. As with any switching buck converter, this capacitor supplies high pulsating currents. The ripple current and ripple voltage can be calculated for the appropriate capacitor using Equation 2 for an approximation:

$$I_{RMS} = I_{OUT} \times \sqrt{D\,(1 - D)} \qquad \textbf{Equation 2}$$

$$\text{where } D = \frac{V_{OUT}}{V_{IN}}$$

The voltage ripple across the input ceramic capacitor is given by Equation 3:

$$V_{PP} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{C_{PVIN} \times f_{SW}} \right) \qquad \textbf{Equation 3}$$

For typical application as described in Table 4, assuming a maximum load current of 6A, the ripple current through the capacitor equates to I_{RMS} = 2.24A. When the recommended 2 x 10µF PVIN capacitor is used, the voltage ripple is calculated to be 21mV_{PP}. This calculation excludes the effect of series inductance in the capacitor and the PCB trace leading to it. In actual applications, the PVIN voltage spikes caused by this inductance way exceed the calculated ripple voltage. Therefore, it is recommended that two 10µF capacitors be used instead of a single 22µF. Additionally, it is recommended that 10V capacitors be used for PVIN = 5V applications and 25V capacitors be used when the PVIN voltage is 6V to 8.4V.

7.2.3 Output Capacitor – C_{OUT}

The output capacitor temporarily supplies the transient load current as well as provides regulator stability. For stability, the minimum C_{OUT} should be approximately150µF per phase, and this should provide a reasonable load step response. This value can be increased to reduce the voltage droop due to load transients but with diminishing effect. The capacitance can be provided from the load device's supply bypass capacitor bank, depending upon a few considerations. In general, for converter stability, the feedback should be taken across the output capacitor C_{OUT}.

For most systems, the host PMIC's buck converter feedback and ground-sense signals will be connected at the load device's power supply pins and ground connection points respectively, where the supply capacitor bank is usually also placed. The voltage dependency of the capacitor, which can vary with case size, should be such that the de-rated capacitance is at least 141µF per DPU of total capacitance in the bank. In this case, the local C_{OUT} at each DPU may be removed. Recommendation: In the case of a distributed power system where the individual DPUs are widely separated on the PCB or far away from the load device, add an additional 10µF ceramic capacitor placed locally at the V_{OUT} side of the inductor connection of each DPU. This local capacitor will absorb some of the inductor ripple current, reducing EMI effects in the PCB trace connecting V_{OUT} to the load device.

7.2.4 VPG Bypass Capacitor – C_{VPG}

C_{VPG} is the decoupling capacitor for the internal 4.8V high-side LDO that supplies the high-side switch driving circuitry, and it is connected between the PVIN and VPG pins. A 10V 2.2µF ceramic capacitor should be used. The voltage dependency of the capacitor, which can vary with case size, should be such that the de-rated capacitance is at least 1.8µF when 4.8V is across it.

7.2.5 VSYS Bypass Capacitor – C_{VSYS}

C_{VSYS} is the decoupling capacitor for the internal 4.8V low-side LDO that supplies the low-side switch driving circuitry, and it is connected between the VSYS pin and the PGND EPAD. A 10V 2.2µF ceramic capacitor of the same type used for C_{VPG} should be used for C_{VSYS} as well.

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7.2.6 ID and Configuration Setting Resistor – R_{SET}

The R_{SET} resistor is used to configure the P9148 with an individual identifier (ID). The identifier ensures that each device can be correctly addressed by the host PMIC. The device ID should be assigned in an ascending order starting with ID0, as the ID determines the switching phase position of the DPU. This ensures the output ripple is minimized as the switching phases of all attached DPUs are automatically distributed uniformly in time. With respect to the output ripple, this effectively scales up the equivalent switching frequency by the number of DPUs present. To ensure uniform phase distribution, the DPUs must know if they are attached to buck rails with integrated power stages (DCD0, DCD1, DCD2) on the host PMIC or to standalone controllers (DCD3, DCD4) within the PMIC. In the case when they are connected to an existing buck rail, the PMIC's integrated power stage will provide one of the switching phases. This information is also derived from the R_{SET} resistor value.

One or more DPUs can be set to an identical ID using the same R_{SET} resistor value. In this case, the advantage of phase spreading (multi-phase) is lost since DPUs with identical ID will switch at the same time.

In addition to the device ID and the controller mode setting, the R_{SET} resistor can also be used to configure the slope compensation setting of the device as shown in Table 7.

Table 7. Recommended R_{SET} Values

Type of Buck Rails	R_{SET} [kΩ]	Slope Compensation	ID
For DCD0, DCD1, and DCD2	1.0	LOW	0
	6.65	LOW	1
	13.3	LOW	2
	20.0	LOW	3
	26.7	HIGH	0
	33.2	HIGH	1
	40.2	HIGH	2
	46.4	HIGH	3
For DCD3 and DCD4	53.6	LOW	0
	60.4	LOW	1
	66.5	LOW	2
	73.2	LOW	3
	80.6	HIGH	0
	86.6	HIGH	1
	93.1	HIGH	2
	100	HIGH	3

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8. PCB Layout Considerations

8.1 DIO and DIF Communication Lines

The DIO and DIF signals transition at a controlled edge rate of typically 8ns with a driving impedance of 70Ω. In most applications, these lines do not need to be treated as transmissions lines, but it is recommended to use trace widths for a Z_0 of approximately 70Ω for optimum signal integrity. In the case when DPUs are widely distributed (e.g., at the 4 corners of the load device), avoid branching or using star-connections on the DIO and DIF lines as this might cause signal degradation due to unnecessary reflections at branch points.

8.2 C_{OUT} Placement

All C_{OUT} capacitors should be clustered together and placed as close to the load device as possible. The feedback voltage and ground sense lines of the host PMIC should be connected across the load capacitor bank.

For optimum device performance, the following guidelines should be observed. Contact IDT for Gerber files that contain the recommended board layout.

- The C_{VSYS} and C_{VPG} decoupling capacitors should be mounted on the component side of the board, close to their respective pins. Recommendation: Do not use vias between the decoupling capacitors and their pins and keep their PCB traces as short as possible. Due to the high switching currents possible and the high input voltage range, the C_{PVIN} mounting inductance should be less than the C_{PVIN} capacitor's ESL, which is approximately 1nH. This can be accomplished by placing C_{PVIN} as shown in section 9, using only the top layer route to connect to the PVIN pins and the PGND EPAD, minimizing inductance in the PVIN-PGND loop.
- If the PVIN plane or the ground plane is not the top layer, then vias can be used outside of the PVIN-PGND loop to connect the P9148 to those planes. Since the C_{PVIN} capacitor case size can easily allow a 4-via connection, this should be used. For the PGND EPAD connection, the number of vias connecting the PGND EPAD to the ground plane should be maximized for thermal consideration. It is recommended that at least 10 vias are used for this connection for typical applications.
- The 12-DFN package has an inner thermal pad, which requires blind assembly. It is recommended that a more active flux solder paste be used such as the Alpha OM-350 solder paste (https://alphaassembly.com/Products/Solder-Paste/OM-350). Contact IDT for Gerber files that contain a recommended solder stencil design.
- The package center exposed pad (EPAD) must be reliably soldered directly to the PCB. The center land pad on the PCB (set 1:1 with EPAD) must also be tied to the board ground plane, primarily to maximize thermal performance in the application. The ground connection is best achieved using a matrix of plated-through-hole (PTH) vias embedded in the PCB center land pad. The PTH vias perform as thermal conduits to the ground plane (thermally, a heat spreader) as well as to the solder side of the board. Recommendations for the via finished hole-size and array pitch are 0.3mm to 0.33mm and 1.3mm, respectively.
- The PCB design and layout can have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces and planes to transfer heat away from the package. The following general guidelines will be helpful in designing a board layout for low thermal resistance:
    1. PC board traces with large cross sectional areas have higher thermal conductivity. If possible, a 2oz copper ground plane with ample thermal vias connecting to the EPAD of the P9148 is recommended.
    2. Do not use solder mask or place silkscreen on the heat-dissipating traces/pads, as they increase the net thermal resistance of the mounted IC package.

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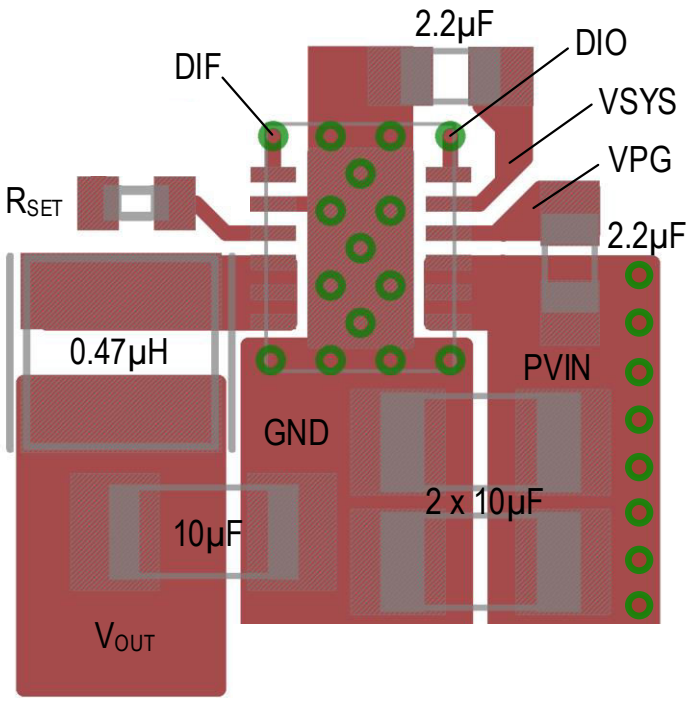
9. Recommended Board Layout

Note that the example layout in Figure 4 shows a 10µF local C_{OUT} configuration that is used in the case of widely separated DPU placements, where the main C_{OUT} capacitor cluster is located far away.

Figure 4. Recommended Board Layout of One DPU



10. Power Dissipation/Thermal Requirements

In addition to layout techniques described in the previous section, placement of the P9148 DPUs with respect to proximity to other heat generating devices should be considered as well. System-dependent considerations, such as thermal mounting, airflow, heat sinking, and convection surfaces, will affect the final power dissipation limit of the P9148 in the application. The main PCB factors influencing θ_{JA} (in the order of decreasing influence) are the number of copper layers, the number of thermal vias connecting the device EPAD to the ground plane, and the ground plane thickness.

The maximum power dissipation for a given situation can be calculated with Equation 4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \qquad \textbf{Equation 4}$$

where: $P_{D(MAX)}$ = Maximum Power Dissipation (W)

θ_{JA} = Package Thermal Resistance (°C/W)

$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The maximum operating junction temperature ($T_{J(MAX)}$) of the P9148 is 125°C. The thermal resistance of the 12-DFN package is optimally θ_{JA} = 36°C/W. Operation is specified for the maximum ambient temperature (T_A) of 85°C. The maximum power dissipation can be calculated with Equation 5.

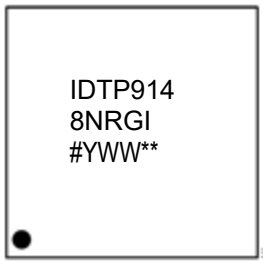
$$P_{D(MAX)} = \frac{(125°C - 85°C)}{36°C/W} = 1.1W \qquad \textbf{Equation 5}$$

11. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/12-dfn-package-outline-drawing-30-x-40-x-09-mm-body-05-mm-pitch-nrnrg12s1-standard

12. Marking Diagram



Line 1: IDT block logo and product name.

Line 2: IDT product name continuation; NRG = package code; I = industrial temperature range.

Line 3: # = product stepping; Y = last character of year assembled; WW = workweek assembled; ** = lot sequence when assembled.

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13. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
P9148NRGI8	3.0 × 4.0 × 0.90 mm 12-DFN package	1	Reel	-40°C to +85°C

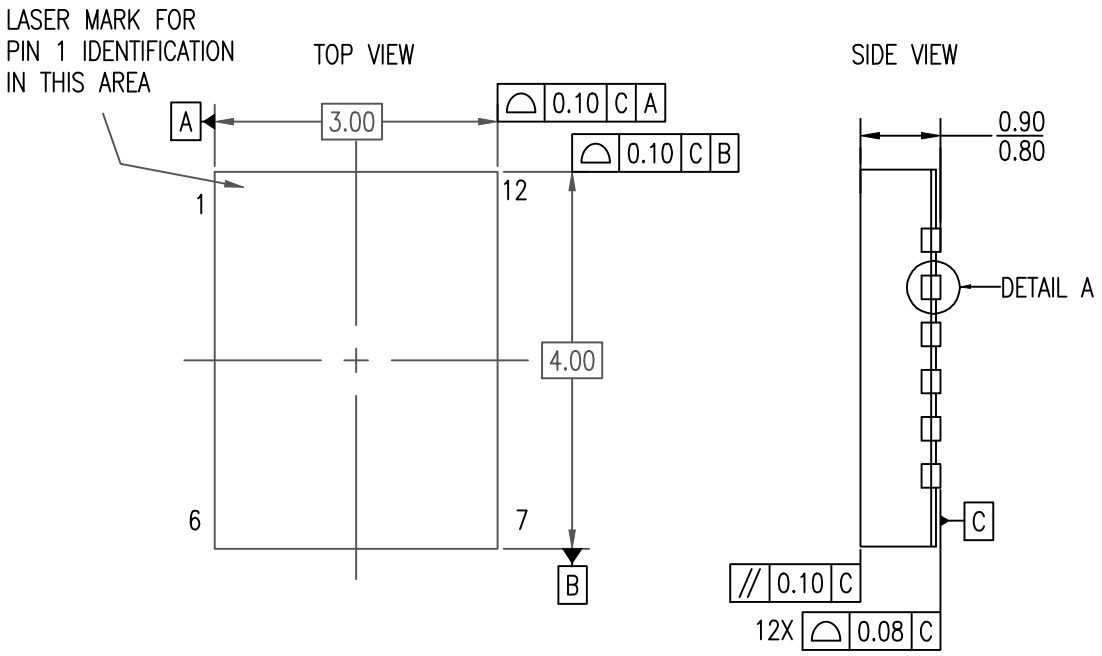
14. Revision History

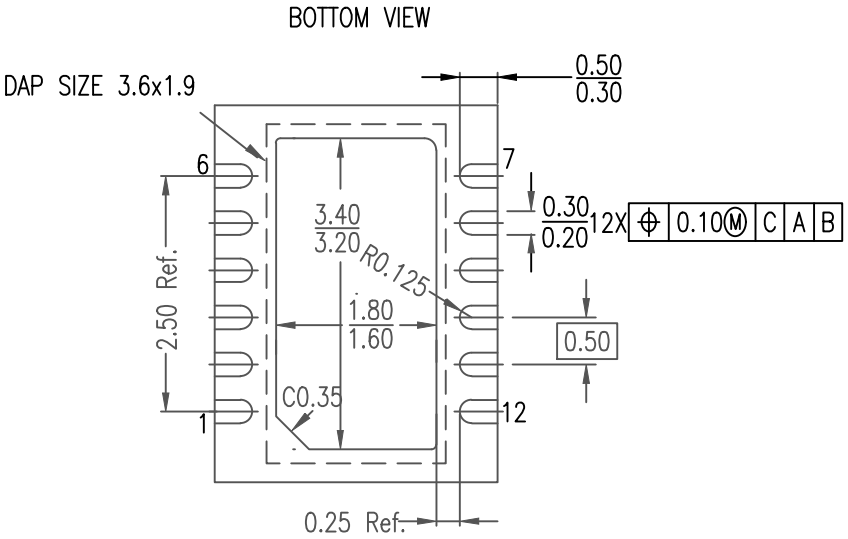
Revision Date	Description of Change
August 1, 2018	▪ Correction for “Condition” column for the LX DC specification in Table 2. – Absolute Maximum Ratings. ▪ Correction for units in Table 3. – Thermal Characteristics. ▪ Correction for symbol in Equation 3. ▪ Minor edits.
June 27, 2018	Initial release.

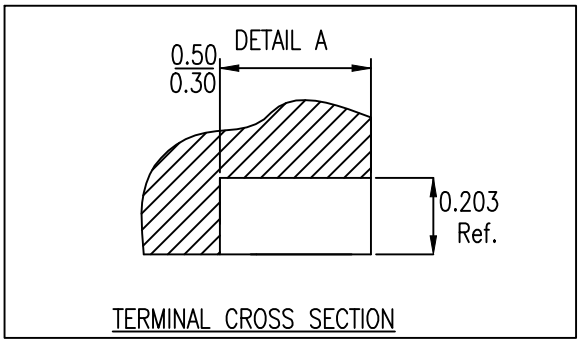
12-DFN Package Outline Drawing

3.0 x 4.0 x 0.9 mm Body, 0.5 mm Pitch

NR/NRG12S1, Standard, PSC-4432-01, Rev 01, Page 1







FINOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DIMENSION & TOLERANCING CONFORM TO ASME Y14.5M–1994
3. THE PIN#1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY

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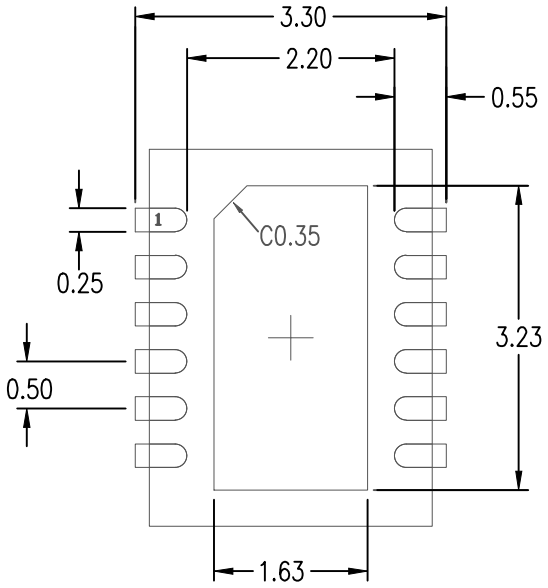

RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM ANGLES IN DEGREES
2. TOP VIEW AS VIEWED IN PCB
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Sept 15, 2017	Rev 01	New POD Format
Mar 24, 2016	Rev 00	Initial Release

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